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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/552,383	04/19/2000	Stephen L. Willis	MICRON.092CP1	3147

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/552,383	WILLIS, STEPHEN L.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *30-37 and 56-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-37 and 56-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 20, 2005 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 33 and 59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear whether the limitation "a BPSG dielectric layer" is further limiting the dielectric layer of a first thickness as recited in the independent claims 30 and 56 or is adding a new layer in addition to the dielectric layer of the first thickness. Clarification is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 30-32, 34-35, 37, 56-58, 60 and 62. are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain et al. (US Pat. No. 5,741,626) in view of Lee et al. (US Pat. No. 6,160,314), and further in view of Sandhu et al. (US Pat. No. 5,069,002).

Regarding claims 30 and 56, Jain et al. teaches a method of forming a dielectric layer of a first thickness on a semiconductor wafer comprising:

forming the dielectric layer (20) of the first thickness on the wafer (12) (see fig. 10);

positioning a sacrificial layer (46) on the dielectric layer (20) (see fig. 10);

forming an aperture (56) in the sacrificial layer (46) and dielectric layer (20) (see fig. 11);

depositing conductive material (58) so as to fill the aperture (56) and so as to be directly in contact with at least a portion of the sacrificial layer (46) (see fig. 12 and col. 6, lines 18-21);

removing the conductive material (58) and the sacrificial layer (46) using a chemical mechanical polishing process (see fig. 12 and col. 6, lines 18-21) ;

However, Jain et al. teaches fails to teach the step of positioning a shield layer between the dielectric layer and the sacrificial layer, wherein the shield layer is formed of a material different than the dielectric layer; and detecting when the CMP process has removed the sacrificial layer.

Lee et al. teaches that it is well known in the art to form a shield layer (206) between the dielectric layer (202) and the sacrificial layer (208) [see fig. 2B], wherein the shield layer (206) is formed of a material different than the dielectric layer (202) (col. 2, lines 48-49 and 54-57).

In addition, Lee et al. teaches that the shield layer (206) is more resistant to planarization by the chemical mechanical polishing process than the sacrificial layer (208) (see col. 3, lines 11-14 and fig. 2C, which shows the shield layer 206 after the CMP); wherein the shield layer inhibits thinning of the dielectric layer during the chemical mechanical polishing process (see col. 3, lines 12-14), and

wherein interposing the sacrificial layer (208) inherently reduces the amount of conductive material on the shield layer (206) following the chemical mechanical polishing process (see fig. 2C); and

halting the chemical mechanical polishing process when the sacrificial layer (208) has been removed (see fig. 2C).

With regards to the "adapted to" limitation, the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. *In re Hutchison* 69 USPQ 138 (CCPA 1946).

The motivation for doing so, as is taught by Lee et al., is to obtain a smoother surface (abstract).

Sandhu et al. teach that is well known in the art to perform a sensing step during the CMP process, in which the change in friction is detected by rotating the wafer and polishing surfaces with electric motors and measuring current changes on one or both of the motors (see abstract and col. 3, lines 38-41 and 55-63 and col. 4, lines 28-30). The motivation for doing so, as is taught by Sandhu et al., is providing a control means for adjusting or stopping the process (abstract).

Jain et al., Lee et al. and Sandhu et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a shield layer between the sacrificial layer and the dielectric layer, wherein the shield layer is more resitant to planarization that the sacrificial layer, inhibits thinning of the dielectric layer during CMP process and reduces the amount of conductive material on the shield layer following the CMP process; and detecting when the CMP process has reached the shield layer and halting the chemical mechanical polishing process upon detecting when the sacrificial layer has been removed and prior to the complete removal of the shield layer so as to maintain the dielectric layer at the first thickness.

Therefore, it would have been obvious to combine Sandhu et al. and Lee et al. with Jain et al. to obtain the invention of claims 30-32, 34-35, 37, 56-58, 60 and 62.

Regarding claims 31-32 and 57-58, Lee et al. teaches that the shield layer (206) is formed of a material (i.e. nitride or aluminum oxide) having a different hardness than the sacrificial layer (208) (i.e. silicon oxide) [col. 2, lines 54-57 and 60-62), and halting the CMP when the shield layer (206) is detected (see fig. 2C); and Sandhu et al. teach that is well known in the art to perform a sensing step during the CMP process, in which the change in friction is detected by rotating the wafer and polishing surfaces with electric motors and measuring current changes on one or both of the motors (see abstract and col. 3, lines 38-41 and 55-63 and col. 4, lines 28-30).

Regarding claim 34, Lee et al. teaches that the CMP process is performed using an etchant selected to remove the sacrificial layer (208) and wherein the shield layer (206) is selected to be resistant to the selected etchant (see fig. 2c and col. 3, lines 9-14).

Regarding claims 35 and 60, Lee et al. teaches that the shield layer (206) is comprised of a nitride layer positioned on the dielectric (202) (see fig. 2B and col. 2, lines 54-57).

Regarding claims 37 and 62, Lee et al. teaches the step of forming a cavity (56) in the dielectric layer (20) and wherein depositing the conductive material (58) on the sacrificial layer (46) results in the cavity being filled with the conductive material (58) (see figs. 11-12 and col. 6, lines 19-22).

6. Claims 33, 36, 59 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain et al. (US Pat. No. 5,741,626) in view of Lee et al. (US Pat. No.

6,160,314) and Sandhu et al. (US Pat. No. 5,069,002), and further in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1: Process Technology, Lattice Press, 1986, pages 189-191).

Regarding claims 33, 36, 59 and 61, Lee et al. teaches that the sacrificial layer (202) is comprised of an oxide layer formed on the shield layer (206) made of silicon oxynitride (DARC material), wherein the shield layer (206) is formed on a lower oxide layer (202) (see fig. 2B and col. 2, lines 48-49, 54-57 and 60-62).

However, the prior art fails to teach that the oxide layers are made of a BPSG glass material. Wolf et al. teaches that BPSG is a very well known oxide material which is commonly used for isolation, passivation, and surface planarization (page 190).

Jain et al., Lee et al., Sandhu et al. and Wolf et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a sacrificial layer made of BPSG glass material, and a BPSG dielectric layer on which the shield layer is formed. The motivation for doing so, as is taught by Wolf et al., is to isolate multilevel structure, provide a good fluidity and coverage step, and reduce stress (fig. 22 and page 190). Therefore, it would have been obvious to combine Wolf et al. with Jain et al., Lee et al. and Sandhu et al. to obtain the invention of claims 33, 36, 59 and 61.

Response to Arguments

7. Applicant's arguments with respect to claims 30-37 and 56-62 have been considered but are moot in view of the new ground(s) of rejection.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/3/07

José R. Díaz
Examiner
Art Unit 2815